

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

5 a gate electrode located over a surface of the substrate and comprising at least first and second elongate wirings which intersect at an intersection region of the gate electrode;

a gate dielectric layer interposed between the gate electrode and the surface of the substrate; and

10 at least one oxide region located in the substrate below the intersection region of the gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer.

15 2. The semiconductor device as claimed in claim 1, wherein the oxide region is a field oxide region.

3. A semiconductor device comprising:

a substrate;

20 a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate;  
and

at least one oxide region located in the substrate  
5 below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer.

4. The semiconductor device as claimed in claim 3,  
10 wherein the mesh-shaped gate electrode comprises a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another, and wherein the first elongate wirings intersect the second elongate wirings to  
15 define an array of gate intersection regions over the surface of the substrate and to further define an array of source/drain regions of the substrate.

5. The semiconductor device as claimed in claim 4,  
20 wherein the at least one oxide region comprises an array of oxide regions located below the array of gate intersection regions, respectively.

6. The semiconductor device as claimed in claim 4,  
25 wherein the at least one oxide region comprises a

plurality of elongate oxide regions extending parallel to each other and lengthwise below the first elongate wirings of the mesh-shaped gate electrode.

5           7. The semiconductor device as claimed in claim 6, wherein each of the plurality of elongate oxide regions have opposite ends which terminate at first and second elongate side oxide regions extending perpendicular to said plurality of elongate oxide regions.

10           8. The semiconductor device as claimed in claim 4, further comprising a common wiring located along at least one side of the array of source/drain regions, wherein each of the first and second elongate wirings are  
15 connected to the common wiring.

          9. The semiconductor device as claimed in claim 8, wherein the common wiring surrounds the array of source/drain regions.

20           10. The semiconductor device as claimed in claim 4, wherein the array of source/drain regions comprises a plurality of spaced apart alternating source and drain regions so that each drain region is surrounded by four

source regions and each source region is surrounded by four drain regions.

11. The semiconductor device as claimed in claim 3,  
5 wherein the at least one oxide region is at least one field oxide region.

12. The semiconductor device as claimed in claim 4,  
further comprising:

10 a dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a plurality of elongate drain electrodes located over the dielectric layer and extending parallel to each other and diagonally over said array of source/drain  
15 regions;

a plurality of elongate source electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain  
regions;

20 wherein said source electrodes are electrically connected through said dielectric layer to source regions among said source/drain regions, and wherein said drain electrodes are electrically connected through said dielectric layer to drain regions among said array of  
25 source/drain regions, and wherein source electrodes and

said drain electrodes are alternately arranged over said dielectric layer.

13. The semiconductor device as claimed in claim 12,  
5 further comprising:

a common source electrode connected to said plurality of source electrodes; and

a common drain electrode connected to said plurality of drain electrodes.

10 14. The semiconductor device as claimed in claim 4, further comprising:

a first dielectric layer formed over the semiconductor substrate and the mesh-shaped gate  
15 electrode;

a plurality of elongate first electrodes located over said first dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

20 a second dielectric layer formed over said first dielectric layer and said first electrodes;

a plurality of elongate second electrodes located over said second dielectric layer and extending parallel to each other and diagonally over said array of  
25 source/drain regions;

wherein said first electrodes are electrically connected through said first dielectric layer to either source or drain regions among said array of source/drain regions, and wherein said second electrodes are  
5 electrically connected through said first and second dielectric layers to the other of source or drain regions among said array of source/drain regions.

15. The semiconductor device as claimed in claim 14,  
10 wherein said first electrodes and said second electrodes are alternately arranged over said substrate.

16. The semiconductor device as claimed in claim 14,  
wherein said first electrodes and said second electrodes  
15 are arranged perpendicularly to each other over said substrate.

17. The semiconductor device as claimed in claim 14,  
further comprising:

20 a common first electrode connected to said plurality of first electrodes; and

a common second electrode connected to said plurality of second electrodes.

18. The semiconductor device as claimed in claim 4,  
further comprising:

a first dielectric layer formed over the  
semiconductor substrate and the mesh-shaped gate  
electrode;

a first mesh-shaped electrode located over said  
dielectric layer, said first mesh-shaped electrode  
comprising a plurality of third elongate wirings  
extending parallel to one another and diagonally over  
said array of source/drain regions, and a plurality of  
fourth elongate wirings extending parallel to one another  
and diagonally over said array of source/drain regions,  
and wherein said third elongate wirings intersect said  
fourth elongate wirings;

a second dielectric layer formed over said first  
dielectric layer and said first mesh-shaped electrode;

a second mesh-shaped electrode located over said  
second dielectric layer, said second mesh-shaped  
electrode comprising a plurality of fifth elongate  
wirings extending parallel to one another and diagonally  
over said array of source/drain regions, and a plurality  
of sixth elongate wirings extending parallel to one  
another and diagonally over said array of source/drain  
regions, and wherein said fifth elongate wirings  
intersect said sixth elongate wirings;

wherein said first mesh-shaped electrode is electrically connected through said first dielectric layer to either source or drain regions among said array of source/drain regions, and wherein said second mesh-shaped electrode is electrically connected through said first and second dielectric layers to the other of source or drain regions among said array of source/drain regions.

19. A semiconductor device comprising:

a substrate;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate, and defining an array of gate intersection regions over the surface of the substrate and an array of source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shaped gate electrode and the surface of the substrate;

and

at least one oxide region located in the substrate below the intersection region of the gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer;



a dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a plurality of elongate first electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

a second dielectric layer formed over said first dielectric layer and said first electrodes;

a plurality of elongate second electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

wherein said first electrodes are electrically connected through said first dielectric layer to either source or drain regions among said array of source/drain regions, and wherein said second electrodes are electrically connected through said first and second dielectric layers to the other of source or drain regions among said array of source/drain regions.

20. The semiconductor device as claimed in claim 19, wherein the at least one oxide region comprises an array of oxide regions located below the array of gate intersection regions, respectively.

21. The semiconductor device as claimed in claim 19, wherein the at least one oxide region comprises a plurality of elongate oxide regions extending parallel to each other.

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22. The semiconductor device as claimed in claim 21, wherein each of the plurality of elongate oxide regions have opposite ends which terminate at first and second elongate side oxide regions extending perpendicular to said plurality of elongate oxide regions.

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23. The semiconductor device as claimed in claim 19, wherein said first electrodes and said second electrodes are alternately arranged over said substrate.

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24. The semiconductor device as claimed in claim 19, wherein said first electrodes and said second electrodes are arranged perpendicularly to each other over said substrate.

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25. The semiconductor device as claimed in claim 19, further comprising a common first electrode connected to said plurality of first electrodes, and a common second electrode connected to said plurality of second electrodes.

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26. The semiconductor device as claimed in claim 19,  
wherein the at least one oxide region is at least one  
field oxide region.

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27. A semiconductor device comprising:

a substrate;

a mesh-shaped gate electrode located over a surface  
of the substrate, the mesh-shaped gate electrode having a  
plurality of openings aligned over respective  
source/drain regions of the substrate;

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a gate dielectric layer interposed between the mesh-  
shape gate electrode and the surface of the substrate;

at least one oxide region located in the substrate  
below the mesh-shaped gate electrode, wherein a thickness  
of the oxide region is greater than a thickness of the  
gate dielectric layer;

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a dielectric layer formed over the semiconductor  
substrate and the mesh-shaped gate electrode;

a plurality of elongate drain electrodes located  
over the dielectric layer and extending parallel to each  
other and diagonally over said array of source/drain  
regions; and

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a plurality of elongate source electrodes located  
over said dielectric layer and extending parallel to each

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other and diagonally over said array of source/drain regions;

wherein source electrodes and said drain electrodes are alternately arranged over said dielectric layer.

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28. The semiconductor device as claimed in claim 27, wherein the at least one oxide region comprises an array of oxide regions located below gate intersection regions of the mesh-shaped gate electrode, respectively.

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29. The semiconductor device as claimed in claim 27, wherein the at least one oxide region comprises a plurality of elongate oxide regions extending parallel to each other and lengthwise below elongate wirings of the mesh-shaped gate electrode.

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30. The semiconductor device as claimed in claim 29, wherein each of the plurality of elongate oxide regions have opposite ends which terminate at first and second elongate side oxide regions extending perpendicular to said plurality of elongate oxide regions.

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31. The semiconductor device as claimed in claim 27, wherein each of the plurality of elongate drain electrodes terminate at one end at a first L-shaped

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common wiring, and each of the plurality of elongate source electrodes terminate at one end at a second L-shaped common wiring.

5           32. The semiconductor device as claimed in claim 27, wherein the elongate drain electrodes and the elongate source electrodes are coplanar.

10           33. The semiconductor device as claimed in claim 27, wherein the at least one oxide region is at least one field oxide region.

          34. A semiconductor device comprising:  
a substrate;  
15       a first mesh-shaped electrode located over a surface of the substrate;  
a first dielectric layer interposed between the first mesh-shaped electrode and the surface of the substrate;  
20       a second dielectric layer formed over the first mesh-shaped electrode;  
a second mesh-shaped electrode located over said second dielectric layer;  
a third dielectric layer formed over the second  
25       mesh-shaped electrode; and

a third mesh-shaped electrode located over said  
third dielectric layer.

35. A semiconductor device as claimed in claim 34,  
5 wherein the first mesh-shaped electrode is gate electrode  
and the first dielectric layer is gate dielectric layer.

36. A semiconductor device as claimed in claim 35,  
wherein the first mesh-shaped electrode includes a  
10 plurality of openings aligned over the substrate and  
defines an array of gate intersection regions over the  
substrate and an array of source/drain regions over the  
substrate.

37. A semiconductor device as claimed in claim 36,  
15 further comprising at least one oxide region located in  
the substrate below the first mesh-shaped electrode,  
wherein a thickness of the oxide region is greater than a  
thickness of the first dielectric layer.

38. A semiconductor device as claimed in claim 37,  
20 wherein the oxide region is a field oxide region.

39. A semiconductor device as claimed in claim 36,  
25 wherein the second mesh-shaped electrode is connected to

one of the source/drain regions and the third mesh-shaped electrode is connected the other of the source/drain regions.